



HTM062A02

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深圳市鑫洪泰电子科技有限公司

Shenzhen Hot Display Technology Co.,Ltd

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1. Basic Specifications

1.1 Display Specifications

1>LCD Display Mode	Mono-TFT , Normal Black VA
2>Viewing Angle	Wide View
3>Driving Method	TFT Active Matrix
4>Interface	8080/6800/4L/3L Interface
5>Backlight:	21 Pcs White/Red/Orange LED (Parallel)
6>Controller/Driver	TBD

1.2 Mechanical Specifications

1>Outline Dimension	165.4(L)x92.4 (W)x5.8(H)mm(Detailed Information refer to LCM Drawing)
2>Active Area	145.0(L)x75.0(W)
3>Pixel Pitch	0.21875(L)x0.21875(W)

2. Absolute Maximum Ratings

Items	Symbol	Condition	Unit
I/O Power Supply Voltage	VDDI	-0.3 ~ 6.0	V
Analog Power Supply Voltage	VDDA	-0.3 ~ 6.5	V
Analog Power Supply Voltage	VDDP	-0.3 ~ 6.0	V
LCD Power Supply Voltage	AVDD, GVDD	7.0	V
	AVCL, GVCL, VCOM	-7.0	V
	VGH - VGL	25	V
MPU Interface Input Voltage	VIN	-0.3 ~ VDDI +0.3	V
Operating Temperature	TOP	-20~+70	° C
Storage Temperature	Tst	-30~+80	° C

3. Electrical Characteristics

3.1 DC Characteristics

Items	Symbol	Rating			Unit	Condition	Applicable pin
		MIN.	TYP.	MAX.			
Operating Voltage	VDDI	2.7	-	5.5	V	External Supply	VDDI
Operating Voltage	VDDA	2.7	-	5.5	V	External Supply	VDDA
Operating Voltage	VDDP	2.7	-	5.5	V	External Supply	VDDP
Operating Voltage	VCCO	-	1.8	-	V	Built-in Power Supply	VCCO
Operating Voltage	AVDDO	6.1	-	9	V	Built-in Power Supply	AVDDO
Operating Voltage	AVCLO	-9	-	-6.1	V	Built-in Power Supply	AVCLO
Operating Voltage	GVDD	3.1	-	6.2	V	Built-in Power Supply	GVDD
Operating Voltage	GVCL	-6.2	-	-3.1	V	Built-in Power Supply	GVCL
Operating Voltage	VGH	8.0	-	19.0	V	Built-in Power Supply	VGH
Operating Voltage	VGL	-15.0	-	-5.0	V	Built-in Power Supply	VGL
Operating Voltage	VCOM	-2.0	-	-0.425	V	Built-in Power Supply	VCOM
Input High -Level Voltage	VIH	0.8VDDI	-	VDDI	V		MPU Interface
Input High -Level Voltage	VIL	VSS	-	0.2VDDI	V		MPU Interface
Output High -Level Voltage	VOH	0.8VDDI	-	VDDI	V	VDDI=2.7V,IOL=1mA	D[7:0]
Output Low -Level Voltage	VOL	VSS	-	0.2VDDI	V	VDDI=2.7V,IOL=1mA	D[7:0]
Input Leakage Current	ILI	-1.0	-	1.0	μA	VIN=VDDI or DGND	MPU Interface

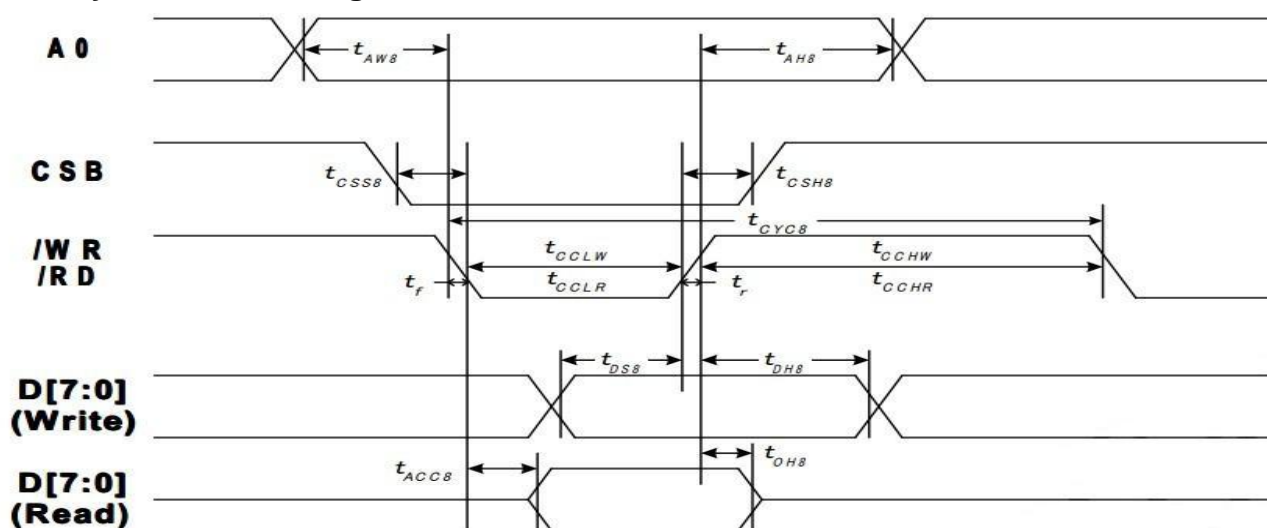
3.2 LED Backlight Circuit

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition	
Average Brightness (without LCD)	IV	TBD	3000	-	cd/m ²	IF=15mA*18	
Operating Temperature	Top	-30	-	80	°C	-	
Storage Temperature	Tst	-40	-	80	°C	-	
Solder Temp. For 3 Seconds	-	-	-	260	°C	-	
Power consumption	Single power	Red	-	140	-	mA	Power =3.3V Ta=25°C
		Orange	-	140	-	mA	
		White	-	330	-	mA	
	Dual power	Red	-	60	-	mA	Power=3.3V BLV =6.0V
		Orange	-	60	-	mA	
		White	-	100	-	mA	



3.3 AC Characteristics

3.3.1 System Bus Timing for 8080 Series MPU



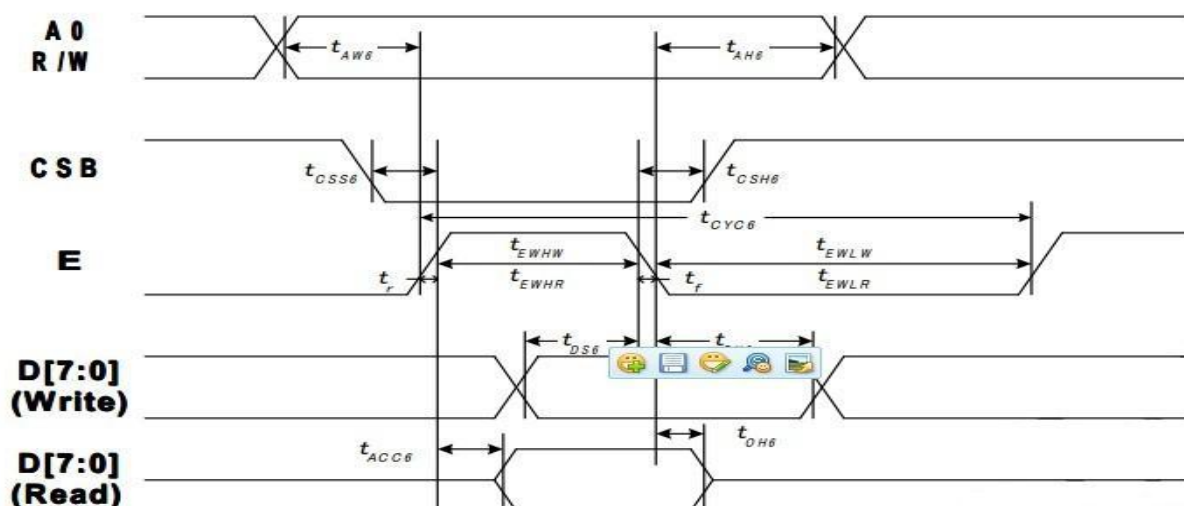
AGND=PGND=DGND=0V, VDDA=VDDP=VDDI=3.0~5.0V, Ta=25° C

Item	Signal	Symbol	Condition	Min	Max	Unit	
Address setup time	AO	tAW8		10	-	ns	
Address hold time		tAH8		0	-		
System cycle time	/WR	TCYC8		1100	-		
/WR L pulse width(WRITE)		TCCLW		500	-		
/WR H pulse width(WRITE)		TCCHW		500	-		
/RD L pulse width(READ)		/RD	TCCLR		950		-
/RD H pulse width(READ)			TCCHR		500		-
CSB setup time		CSB	TCSS8		100		-
CSB hold time	TCSH8			100	-		
WRITE Data setup time	D[7:0]	TDS8		200	-		
WRITE Data hold time		TDH8		50	-		
READ access time		TACC8	CL=100pF	-	950		
READ Output disable time		TOH8	CL=100pF	5	200		

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, $(tr + tf) \leq (tCYC8 - tCCLW - tCCHW)$ for $(tr + tf) \leq (tCYC8 - tCCLR - tCCHR)$ are specified.
2. All timing is specified using 20% and 80% of VDDI as the reference.
3. tCCLW and tCCLR are specified as the overlap between CSB being "L" and /WR and /RD being at the "L" level. CSB and /WR (or /RD) cannot act at the same time and CSB should be 100ns wider than /WR (or /RD).

3.3.2 System Bus Timing for 6800 Series MPU



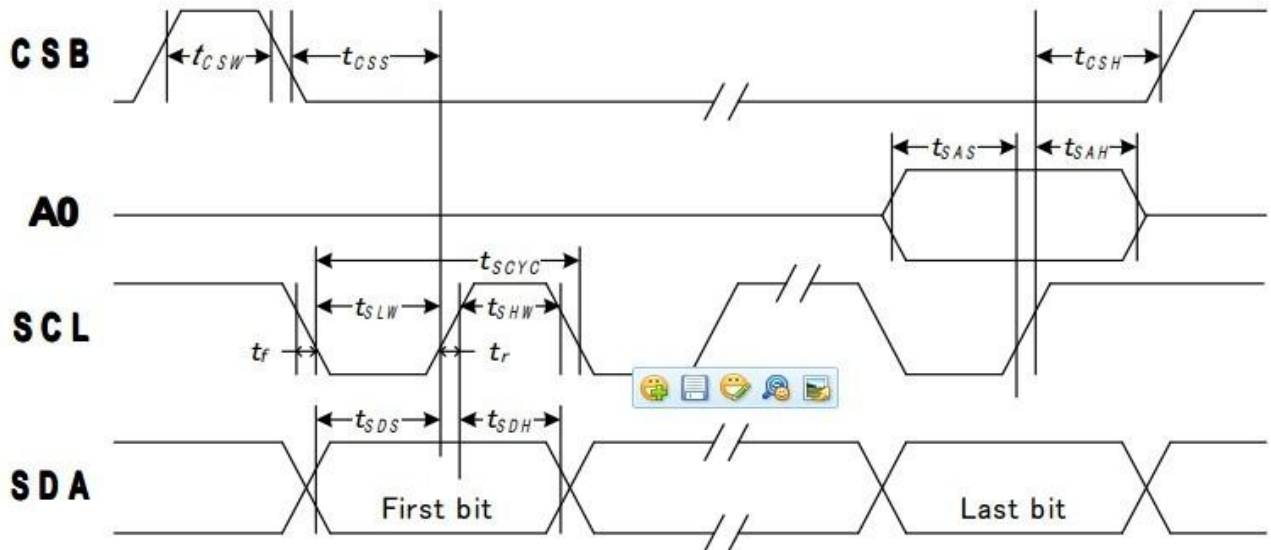
AGND=PGND=DGND=0V, VDDA=VDDP=VDDI=3.0~5.0V, Ta=25° C

Item	Signal	Symbol	Condition	Min	Max	Unit	
Address setup time	AO	TAH6		10	-	ns	
Address hold time		TAH6		0	-		
System cycle time	E	TCYC6		1100	-		
Enable L pulse width(WRITE)		TEWLW		500	-		
Enable H pulse width(WRITE)		TEHWH		500	-		
Enable L pulse width(READ)		TEWLR		500	-		
Enable H pulse width(READ)		TEHWR		500	-		
CSB setup time		CSB	TCSS6		100		-
CSB hold time			TCSH6		130		-
WRITE Data setup time	D[7:0]	TDS6		200	-		
WRITE Data hold time		TDH6		250	-		
Read data access time		TACC6	CL=100pF	-	950		
Read data Output disable time		TOH6	CL=100pF	5	200		

Note:

1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less. When the system cycle time is extremely fast, $(t_r+t_f) \leq (t_{CYC6} - t_{CCLW} - t_{CCHW})$ for $(t_r+t_f) \leq (t_{CYC6} - t_{CCLR} - t_{CCHR})$ are specified.
2. All timing is specified using 20% and 80% of VDDI as the reference.
3. t_{CCLW} and t_{CCLR} are specified as the overlap between CSB being "L" and /WR and /RD being at the "L" level. CSB and /WR (or /RD) cannot act at the same time and CSB should be 100ns wider than /WR (or /RD).

3.3.3 System Bus Timing for 4-Line Series Interface



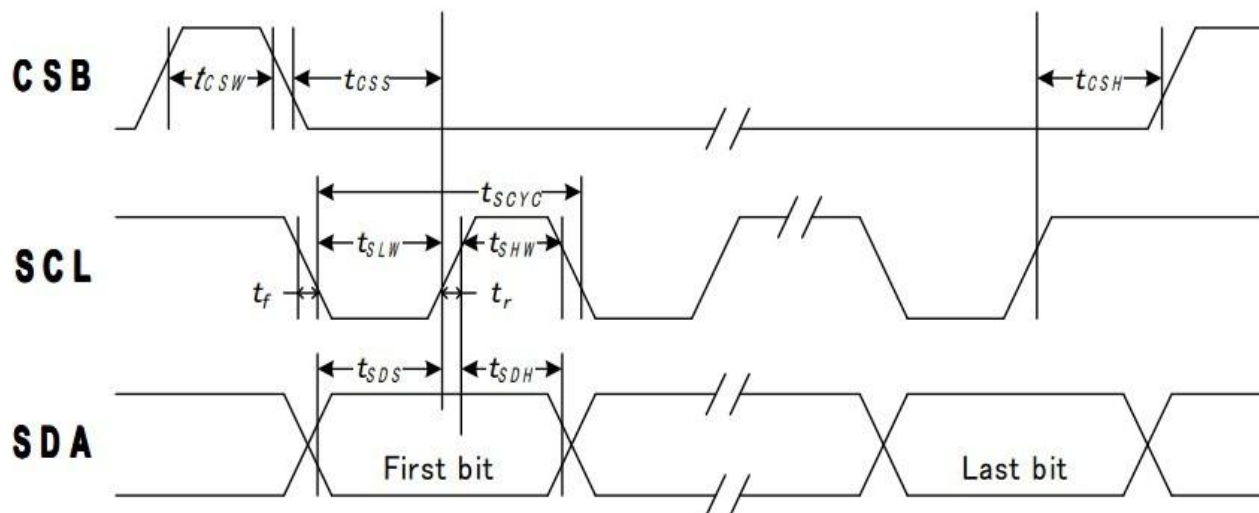
AGND=PGND=DGND=0V, VDDA=VDDP=VDDI=3.0~5.0V, Ta=25° C

Item	Signal	Symbol	Condition	Min	Max	Unit
Serial clock period	SCL	t _{SCYC}		300	-	ns
SCL "H" pulse width		t _{SHW}		150	-	
SCL "L" pulse width		t _{SLW}		150	-	
Address setup time	AO	t _{SAS}		150	-	
Address hold time		t _{SAH}		150	-	
Data setup time	SDA	t _{SDS}		120	-	
Data hold time		t _{SDH}		120	-	
CSB -SCL time	CSB	t _{CSS}		150	-	
CSB-SCL time		t _{CSH}		150	-	
COB"H" Pulse width		t _{CSW}		30	-	

Note:

1. The input signal rise and fall time (tr,tf)arespecifiedat15nsorless.
2. All timing is specifiedusing20%and80% of VDDI as the standard.

3.3.4 System Bus Timing for 3-Line Series Interface



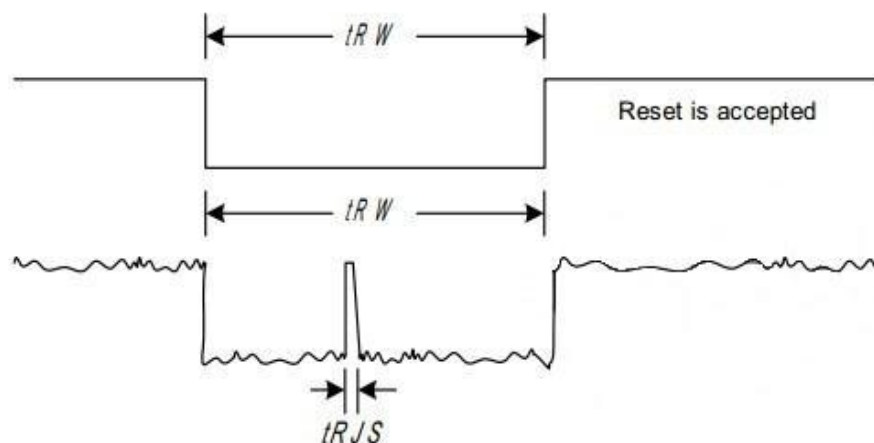
AGND=PGND=DGND=0V, VDDA=VDDP=VDDI=3.0~5.0V, Ta=25° C

Item	Signal	Symbol	Condition	Min	Max	Unit
Serial clock period	SCL	tSCYC		300	-	ns
SCL "H" pulse width		tSHW		150	-	
SCL "L" pulse width		tSLW		150	-	
Data setup time	SDA	tSDS		120	-	
Data hold time		tSDH		120	-	
CSB -SCL time	CSB	tCSS		150	-	
CSB-SCL time		tCSH		150	-	
COB"H" Pulse width		tCSW		30	-	

Note:

1. The input signal rise and fall time (tr,tf) are specified at 15ns or less.
2. All timing is specified using 20% and 80% of VDDI as the standard.

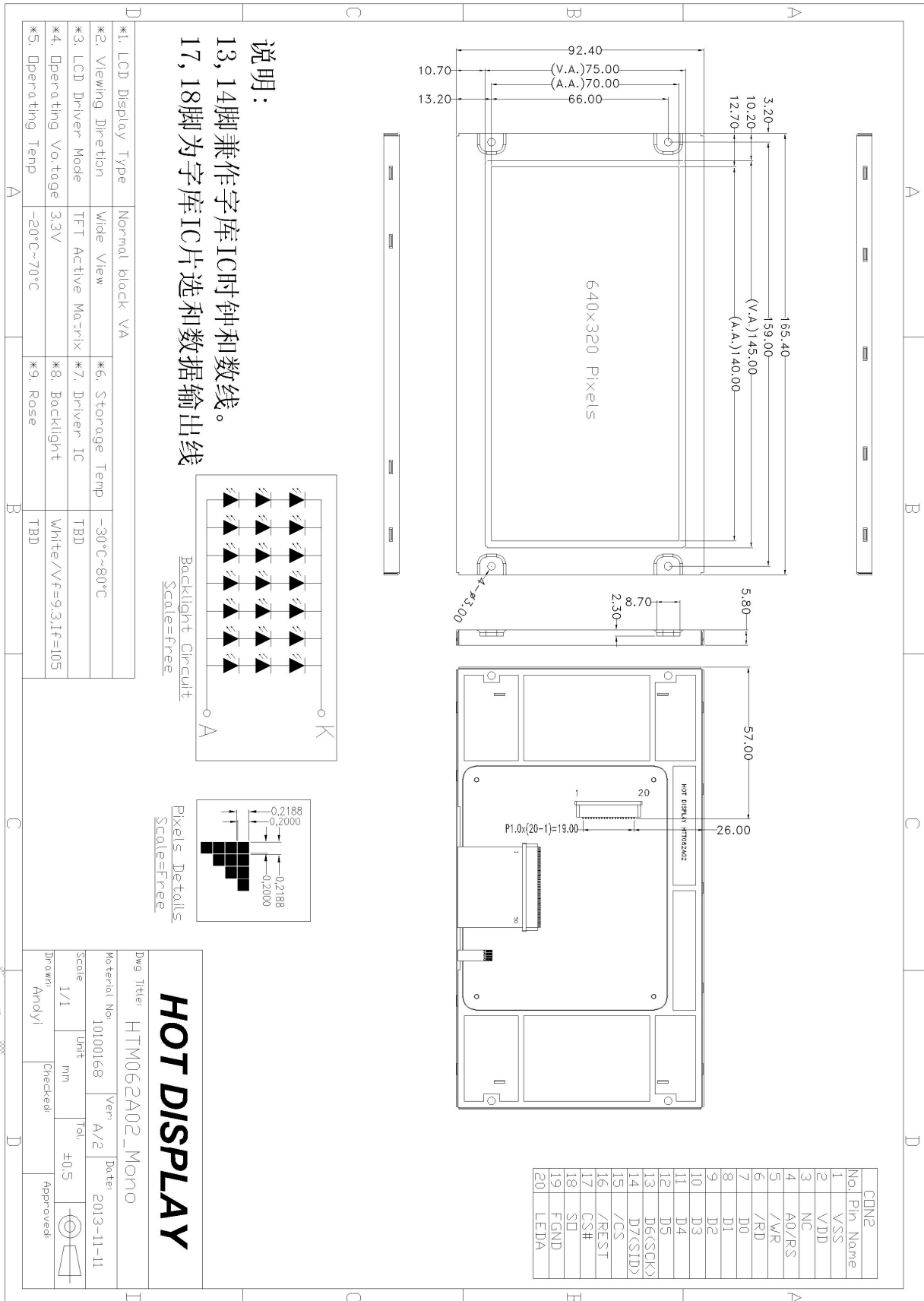
3.4 Rest Timing



Note:

1. For PROM related operation, it takes 50ms at least for PROM Registers to load PROM contents.
Do NOT use any PROM related command during this period
2. When the system issues a RSTB LOW pulse, the reset procedure of IC will start if the LOW pulse is longer than t_{RW} specified above. If the LOW pulse is less than t_{RJS} specified above, the reset procedure of IC will not start.
If the LOW pulse is longer than t_{RJS} and less than t_{RW} , the reset procedure of IC is not guaranteed.

4. Structure Block



4.1 Terminal Function

Pin No.	Pin Name	Typ	Function												
1	VSS		Ground												
2	VDD		Power Supply (3.3V)												
3	NC		NC												
4	RS(A0)		Data /Command identification pin. A0= Hi: Display data or parameter A0=Low: Command When using 3-line serial interface: A0=Hi												
5	ERD	I	Read/ Write execution control pin.When IF1 is 0												
			<table border="1"> <thead> <tr> <th>IF0</th> <th>MPU Type</th> <th>RWR</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>6800 series</td> <td>E</td> <td>Read/Write control input pin. R/W="H": When E is "H",D[7:0] are in output mode. R/W="L":Signals on D[7:0] are latched at the falling edge of E signal.</td> </tr> <tr> <td>0</td> <td>8080 series</td> <td>/RD</td> <td>Read enable input pin. When/ RD is "L", D[7:0] are in Output mode</td> </tr> </tbody> </table>	IF0	MPU Type	RWR	Description	1	6800 series	E	Read/Write control input pin. R/W="H": When E is "H",D[7:0] are in output mode. R/W="L":Signals on D[7:0] are latched at the falling edge of E signal.	0	8080 series	/RD	Read enable input pin. When/ RD is "L", D[7:0] are in Output mode
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			1	6800 series	E	Read/Write control input pin. R/W="H": When E is "H",D[7:0] are in output mode. R/W="L":Signals on D[7:0] are latched at the falling edge of E signal.									
0	8080 series	/RD	Read enable input pin. When/ RD is "L", D[7:0] are in Output mode												
ERD is not used in serial interface and should fix to"R3=0Ω"by VDDI.															
6	RWR	I	Read /Write execution control pin.When IF1 is 0												
			<table border="1"> <thead> <tr> <th>IF0</th> <th>MPU Type</th> <th>RWR</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>6800 series</td> <td>R/W</td> <td>Read/ Write control input pin. R/W="H": read. R/W="L": write.</td> </tr> <tr> <td>0</td> <td>8080 series</td> <td>/WR</td> <td>Write enable input pin. Signals on D[7:0] will be latched at the rising Edge of/ WR signal.</td> </tr> </tbody> </table>	IF0	MPU Type	RWR	Description	1	6800 series	R/W	Read/ Write control input pin. R/W="H": read. R/W="L": write.	0	8080 series	/WR	Write enable input pin. Signals on D[7:0] will be latched at the rising Edge of/ WR signal.
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			1	6800 series	R/W	Read/ Write control input pin. R/W="H": read. R/W="L": write.									
0	8080 series	/WR	Write enable input pin. Signals on D[7:0] will be latched at the rising Edge of/ WR signal.												
RWR is not used in serial interface and should fix to IF1 by VDDI.															
RWR is not used in serial interface and should fix to IF1 by VDDI.															
7~14	D0~D7	I/O	When using 8-bit parallel interface:(6800 or 8080 mode) 8-bit bi-directional data bus.Connect to the data bus of 8-bit microprocessor. When chip select pins are not active(CSB="H"),D[7:0] pins are high impedance.												

		I/O	When using serial interface: 3-line or 4-line D7: Serial input clock(SCL). D0: Serial data (SDA). D[6:1]: fix to“H”by VDDI. When chip select pin (CSB) is not active,D[7:0] are high impedance
15	CSB	I	Chip select input pin. Interface access is enabled when CSB is “H”in Parallel ,SPI interface. When CSB is non-active(CSB=“H”),D[7:0] pins are high impedance.
16	RSTB		Reset input pin.Active when it is low.This pin is Effective when RSTEN pin is High. Initialization is executed when this pin is set to Low.SWRESET command must be required after initialization.
17	CS#		Chip select input pin for GT32L
18	SO		Serial data output pin for GT32L
19	FGND		Equipment grounding
20	LEDA		Backlight Power

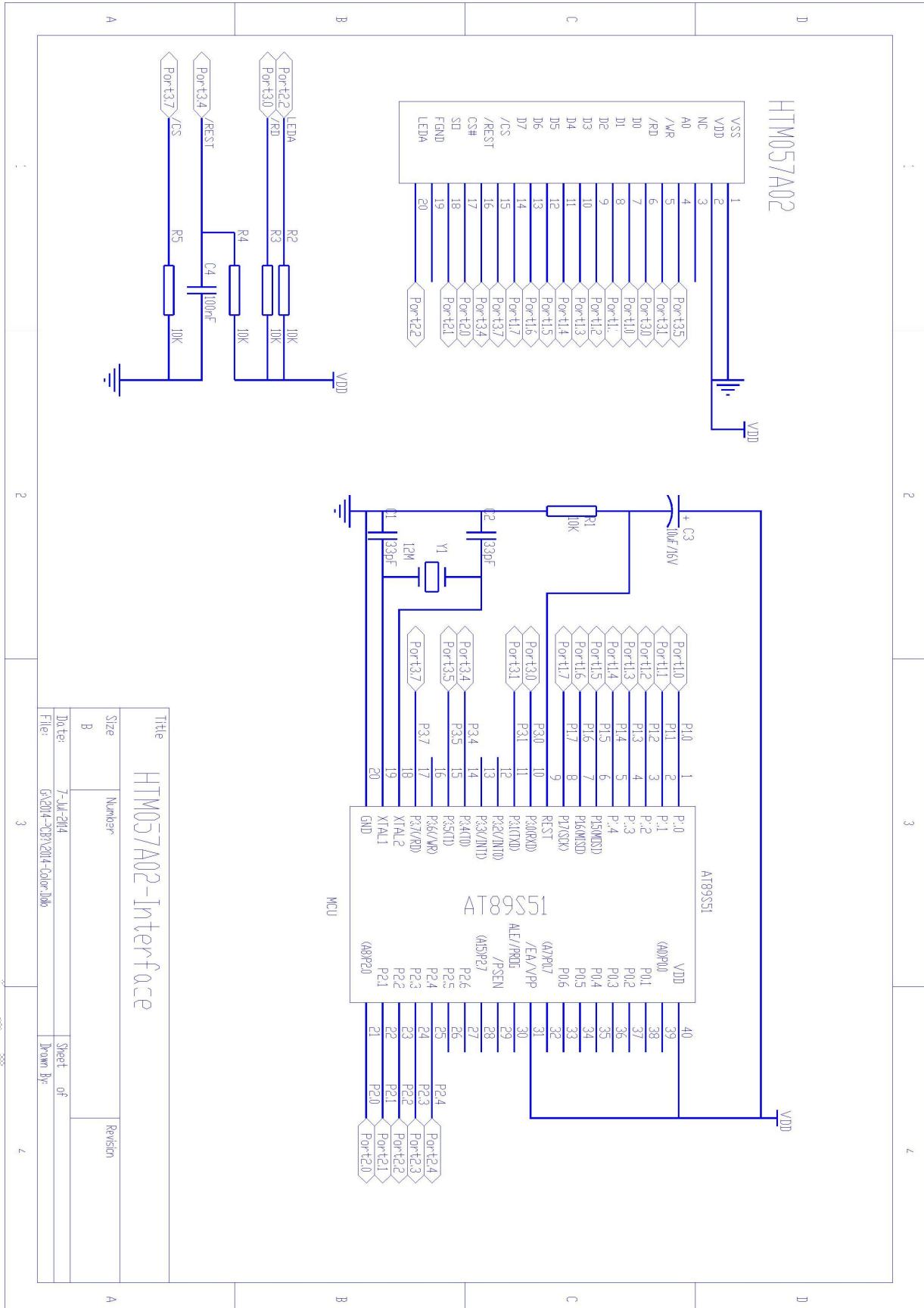
4.2 Interface selection

IF0		IF1		Selected Interface
R1=0R,R2=NC	0	R3=NC,R4=0R	0	8-bit 8080 parallel interface
R1=NC,R2=0R	1	R3=NC,R4=0R	0	8-bit 6800 parallel interface
R1=0R,R2=NC	0	R3=0R,R4=NC	1	3-line serial interface
R1=NC,R2=0R	1	R3=0R ,R4=NC	1	4-line serial interface

4.3 Voltage selection

PX2SET		AVDD pump multiplier	Description
R6=0Ω,R5=NC	1	X2	VDDA=5.0V
R6=NC,R5=0Ω	0	X3	VDDA=3.3V

4.4. Interface specifications



Title		HTM057A02-Interface	
Size	Number	Revision	
B			
Date:	7-Jul-2014	Sheet	of
File:	GA2014-C012014-Color10b	Drawn By	

5. Display Data RAM (DDRAM)

5.1 4bpp DDRAM Map

Page address		0	1	2	...	637	638	639	normal	Column address
normal	invert	639	638	637	...	2	1	0	invert	
0	159	D[0:3]	D[0:3]	D[0:3]	...	D[0:3]	D[0:3]	D[0:3]	G0	
		D[4:7]	D[4:7]	D[4:7]	...	D[4:7]	D[4:7]	D[4:7]	G1	
1	158	D[0:3]	D[0:3]	D[0:3]	...	D[0:3]	D[0:3]	D[0:3]	G2	
		D[4:7]	D[4:7]	D[4:7]	...	D[4:7]	D[4:7]	D[4:7]	G3	
...	
158	1	D[0:3]	D[0:3]	D[0:3]	...	D[0:3]	D[0:3]	D[0:3]	G316	
		D[4:7]	D[4:7]	D[4:7]	...	D[4:7]	D[4:7]	D[4:7]	G317	
159	0	D[0:3]	D[0:3]	D[0:3]	...	D[0:3]	D[0:3]	D[0:3]	G318	
		D[4:7]	D[4:7]	D[4:7]	...	D[4:7]	D[4:7]	D[4:7]	G319	
Source		S0	S1	S2	...	S637	S638	S639	Gate	

Gate	4bpp mode (>160 lines)		4bpp mode (<=160 lines)		2bpp mode		1bpp mode				
	Page address	Frame address	Page address	Frame address	Page address	Frame address	Page address	Frame address			
G0	0	0	0	0/1	0	0/1	0	0/1/2/3			
G1											
G2											
G3	1		1		1		0				
G4	2		2								
G5	3		3								
G6	3		4		4		0/1		0/1	1	0/1/2/3
G7											
G8											
G9	4	4	2	0/1	0/1	1	0/1/2/3				
G10	155	0	75					0/1	0/1	38	0/1/2/3
G11			76								
G12	156	0	77	0/1	0/1	39	0/1/2/3				
G13			78								
G14	157	0	79	0/1	0/1	39	0/1/2/3				
G15			79								
G16	158	0	79	0/1	0/1	39	0/1/2/3				
G17			79								
G18	159	0	79	0/1	0/1	39	0/1/2/3				
G19			79								

6. Commands Descriptions

6.1 Software Reset

AEH	Software Reset											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	1	↑	1	0	1	0	1	1	1	0	AE
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	. This command make a reset as same ad hardware . . It is required Hardware reset at power-on reset . It is always required to input this command after hardware reset											

6.2 Power Control

61H	Power Control											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCTL	0	1	↑	0	1	1	0	0	0	0	0	61
1st parameter	1	1	↑	BST3SR	BST3SR	0	0	FOF40	FOF30	FOF20	FOF10	40
				1	0			N	N	N	N	
2nd parameter	1	1	↑	FOFNO	FOFNO	FOFNO	FOFNO	0	SAMPS	SAMPS	SAMPS	04
				3	2	1	0		et2	et1	et0	
3rd parameter	1	1	↑	0	0	1	0	0	0	1	0	02
4th parameter	1	1	↑	1	0	0	0	0	1	0	1	A5
Description	. Booster circuit control, source amp setting and booster clock frequency settings. . This command must be input before SLPOUT command. . BST3SR[1:0]: Step-up rate of the 3 rd booster setting 00,01:"-1" 10:"-2" 11:"-3" . BST4ON~BST1ON:4th~1st booster On/OFF setting 0:Booster off 1:Booster on . FOFNo[3:0]: Force off frame, set waiting time by number of frames from sleep out to display on. . SAMPSst[2:0]: Source amplifier setting											

6.3 Electronic Volumn Set 1

62H	Electronic Volumn Set 1																																																																																	
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																						
EVSwt1	0	1	↑	0	1	1	0	0	0	1	0	62																																																																						
1st parameter	1	1	↑	0	VCOM6	VCOM5	VCOM4	VCOM3	VCOM2	VCOM1	VCOM0	0A																																																																						
2nd parameter	1	1	↑	0	0	VGHRE G5	VGHRE G4	VGHRE G3	VGHRE G2	VGHRE G1	VGHRE G0	06																																																																						
3rd parameter	1	1	↑	0	0	1	VGHRE G4	VGHRE G3	VGHRE G2	VGHRE G1	VGHRE G0	0F																																																																						
4th parameter	1	1	↑	1	0	0	0	0	1	0	1	A5																																																																						
Description	<p>Set each output voltages of built in voltage regulators VGL and VGH are determined by VGHREG and VGLREG . (refer to 6.5)</p> <table border="1" data-bbox="371 750 705 1310"> <thead> <tr> <th>VCOM[6:0]</th> <th>VCOM(V)</th> </tr> </thead> <tbody> <tr><td>00h</td><td>-0.3000</td></tr> <tr><td>01h</td><td>-0.3125</td></tr> <tr><td>02h</td><td>-0.3250</td></tr> <tr><td>03h</td><td>-0.3375</td></tr> <tr><td>...</td><td>....</td></tr> <tr><td>3Dh</td><td>-1.6025</td></tr> <tr><td>3Eh</td><td>-1.0750</td></tr> <tr><td>3Fh</td><td>-1.0875</td></tr> <tr><td>....</td><td>...</td></tr> <tr><td>7Dh</td><td>-1.8625</td></tr> <tr><td>7Eh</td><td>-1.8750</td></tr> <tr><td>7Fh</td><td>-1.8875</td></tr> </tbody> </table> <table border="1" data-bbox="863 750 1270 1314"> <thead> <tr> <th>VGHREG[5:0]</th> <th>VGHREG(V)</th> </tr> </thead> <tbody> <tr><td>00h</td><td>0</td></tr> <tr><td>01h</td><td>1.5</td></tr> <tr><td>02h</td><td>1.6</td></tr> <tr><td>03h</td><td>1.7</td></tr> <tr><td>...</td><td>...</td></tr> <tr><td>2Eh</td><td>6.0</td></tr> <tr><td>2Fh</td><td>6.1</td></tr> <tr><td>30h</td><td>6.2</td></tr> <tr><td>31h</td><td>6.2</td></tr> <tr><td>...</td><td>...</td></tr> <tr><td>3Eh</td><td>6.2</td></tr> <tr><td>3Fh</td><td>6.2</td></tr> </tbody> </table> <table border="1" data-bbox="413 1440 820 1825"> <thead> <tr> <th>VGHREG[4:0]</th> <th>VGHREG(V)</th> </tr> </thead> <tbody> <tr><td>00h</td><td>2.4</td></tr> <tr><td>01h</td><td>2.5</td></tr> <tr><td>02h</td><td>2.6</td></tr> <tr><td>03h</td><td>2.7</td></tr> <tr><td>...</td><td>...</td></tr> <tr><td>1Dh</td><td>5.3</td></tr> <tr><td>1Eh</td><td>5.4</td></tr> <tr><td>1Fh</td><td>5.5</td></tr> </tbody> </table>												VCOM[6:0]	VCOM(V)	00h	-0.3000	01h	-0.3125	02h	-0.3250	03h	-0.3375	3Dh	-1.6025	3Eh	-1.0750	3Fh	-1.0875	7Dh	-1.8625	7Eh	-1.8750	7Fh	-1.8875	VGHREG[5:0]	VGHREG(V)	00h	0	01h	1.5	02h	1.6	03h	1.7	2Eh	6.0	2Fh	6.1	30h	6.2	31h	6.2	3Eh	6.2	3Fh	6.2	VGHREG[4:0]	VGHREG(V)	00h	2.4	01h	2.5	02h	2.6	03h	2.7	1Dh	5.3	1Eh	5.4	1Fh	5.5
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6.4 Display Set 2

33H	Display Set 2											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISAR	0	1	↑	0	0	1	1	0	0	1	1	33
1st parameter	1	1	↑	SOnT7	SOnT6	SOnT5	SOnT4	SOnT3	SOnT2	SOnT1	SOnT0	0A
2nd parameter	1	1	↑	SOffT7	SOffT6	SOffT5	SOffT4	SOffT3	SOffT2	SOffT1	SOffT0	28
3rd parameter	1	1	↑	GOnT7	GOnT6	GOnT5	GOnT4	GOnT3	GOnT2	GOnT1	GOnT0	0C
4th parameter	1	1	↑	GOffT7	GOffT6	GOffT5	GOffT4	GOffT3	GOffT2	GOffT1	GOffT0	26
Description	. Set source and gate ON/OFF timing . SOnT: Set source on timing by “number of clock from start-1” . SOffT: Set source off timing by “number of clock from start-1” . SOnT: Set source on timing by “number of clock from start-1” . SOffT: Set source off timing by “number of clock from start-1”											

6.5 Electronic Volumn Set 2

63H	Electronic Volumn Set 1																																																											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																
EVSET2	0	1	↑	0	1	1	0	0	0	1	0	63																																																
1st parameter	1	1	↑	0	0	0	GVDD4	GVDD3	GVDD2	GVDD1	GVDD0	0F																																																
2nd parameter	1	1	↑	0	0	0	GVCL4	GVCL3	GVCL2	GVCL1	GVCL0	0F																																																
3rd parameter	1	1	↑	1	0	1						A5																																																
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5																																																
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6.6 Memory Address Control

24H	Memory Address Control											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MADCTL	0	1	↑	0	0	1	0	0	1	0	0	24
1st parameter	1	1	↑	0	0	0	0	0	MV	MY	MX	00
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> ▪ Set about display data TAM. ▪ To access display RAM, it is required 1ms or more wait after input this command. ▪ MV: Select address incremental direction.(refer to 6.) <ul style="list-style-type: none"> 0: Incremental column addr . 1:Incremental page addr. ▪ MY: Display data RAM page address (refer to 6.) <ul style="list-style-type: none"> 0: Normal 1: Reverse ▪ MX: Display data RAM column address (refer to 6.). <ul style="list-style-type: none"> 0: Normal 1: Reverse 											

6.7 BPP Select

22H	BPP Selection											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BPPSEL	0	1	↑	0	0	1	0	0	0	1	0	22
1st parameter	1	1	↑	0	0	0	0	0	0	Bppsel1	Bppsel0	02
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> ▪ Set data format (bit per pixel) ▪ It is enabled next frame after receiving the command. ▪ It is possible to change 4bpp / 2bpp / 1bpp. ▪ It must be input during display off state, and display data must be written after changing ▪ BppSel[1:0] : Set data format (bit per pixel) <ul style="list-style-type: none"> 00: 1bpp (2 gray scale) 01: 2bpp (4 gray scale) 10: 4bpp (16 gray scale) 											

6.8 Gamma Set 4bpp Positive 1

91H	Gamma Set 4bpp Positive 1											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P1	0	1	↑	0	0	0	1	0	0	0	1	91
1st parameter	1	1	↑	0	0	G4BPV0 5	G4BPV0 4	G4BPV0 3	G4BPV0 2	G4BPV0 1	G4BPV0 0	00
2nd parameter	1	1	↑	0	0	G4BPV1 5	G4BPV1 4	G4BPV1 3	G4BPV1 2	G4BPV1 1	G4BPV1 0	04
3rd parameter	1	1	↑	0	0	G4BPV2 5	G4BPV2 4	G4BPV2 3	G4BPV2 2	G4BPV2 1	G4BPV2 0	08
4th parameter	1	1	↑	0	0	G4BPV3 5	G4BPV3 4	G4BPV3 3	G4BPV3 2	G4BPV3 1	G4BPV3 0	0C
Description	<ul style="list-style-type: none"> Set LCD gamma voltage setting of positive polarity in 4bpp mode. This command must be input before SLPOUT. G4BPV0: V0 voltage setting (positive polarity) G4BPV1: V1 voltage setting (positive polarity) G4BPV2: V2 voltage setting (positive polarity) G4BPV3: V3 voltage setting (positive polarity) 											

6.9 Gamma Set 4bpp Positive 2

92H	Gamma Set 4bpp Positive 2											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P2	0	1	↑	1	0	0	1	0	0	1	0	92
1st parameter	1	1	↑	0	0	G4BPV4 5	G4BPV4 4	G4BPV4 3	G4BPV4 2	G4BPV4 1	G4BPV4 0	10
2nd parameter	1	1	↑	0	0	G4BPV5 5	G4BPV5 4	G4BPV5 3	G4BPV5 2	G4BPV5 1	G4BPV5 0	14
3rd parameter	1	1	↑	0	0	G4BPV6 5	G4BPV6 4	G4BPV6 3	G4BPV6 2	G4BPV6 1	G4BPV6 0	18
4th parameter	1	1	↑	0	0	G4BPV7 5	G4BPV7 4	G4BPV7 3	G4BPV7 2	G4BPV7 1	G4BPV7 0	1C
Description	<ul style="list-style-type: none"> Set LCD gamma voltage setting of positive polarity in 4bpp mode. This command must be input before SLPOUT. G4BPV4: V4 voltage setting (positive polarity) G4BPV5: V5 voltage setting (positive polarity) G4BPV6: V6 voltage setting (positive polarity) G4BPV7: V7 voltage setting (positive polarity) 											

6.10 Gamma Set 4bpp Positive 3

93H	Gamma Set 4bpp Positive 3											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P3	0	1	↑	1	0	0	1	0	0	1	1	93
1st parameter	1	1	↑	0	0	G4BPV8 5	G4BPV8 4	G4BPV8 3	G4BPV8 2	G4BPV8 1	G4BPV8 0	23
2nd parameter	1	1	↑	0	0	G4BPV9 5	G4BPV9 4	G4BPV9 3	G4BPV9 2	G4BPV9 1	G4BPV9 0	27
3rd parameter	1	1	↑	0	0	G4BPVA 5	G4BPVA 4	G4BPVA 3	G4BPVA 2	G4BPVA 1	G4BPVA 0	2B
4th parameter	1	1	↑	0	0	G4BPV B5	G4BPV B4	G4BPV B3	G4BPV B2	G4BPV B1	G4BPV B0	2F
Description	<ul style="list-style-type: none"> Set LCD gamma voltage setting of positive polarity in 4bpp mode. This command must be input before SLPOUT. G4BPV8: V8 voltage setting (positive polarity) G4BPV9: V9 voltage setting (positive polarity) G4BPV10: V10 voltage setting (positive polarity) G4BPV11: V11 voltage setting (positive polarity) 											

6.11 Gamma Set 4bpp Positive 4

94H	Gamma Set 4bpp Positive 4											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P4	0	1	↑	1	0	0	1	0	0	1	1	94
1st parameter	1	1	↑	0	0	G4BPV C5	G4BPV C4	G4BPV C3	G4BPV C2	G4BPV C1	G4BPV C0	33
2nd parameter	1	1	↑	0	0	G4BPV D5	G4BPV D4	G4BPV D3	G4BPV D2	G4BPV D1	G4BPV D0	37
3rd parameter	1	1	↑	0	0	G4BPV E5	G4BPV E4	G4BPV E3	G4BPV E2	G4BPV E1	G4BPV E0	3B
4th parameter	1	1	↑	0	0	G4BPVF 5	G4BPVF 4	G4BPVF 3	G4BPVF 2	G4BPVF 1	G4BPVF 0	3F
Description	<ul style="list-style-type: none"> Set LCD gamma voltage setting of positive polarity in 4bpp mode. This command must be input before SLPOUT. G4BPV12: V12 voltage setting (positive polarity) G4BPV13: V13 voltage setting (positive polarity) G4BPV14: V14 voltage setting (positive polarity) G4BPV15: V15 voltage setting (positive polarity) 											

6.12 Sleep Out

12H	Sleep Out											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	1	↑	0	0	0	1	0	0	1	0	12
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> This command make a reset as same as hardware reset. It is required hardware reset at power-on. It is always required to input this command after hardware reset. 											

Sleep In

13H	Sleep Out											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPIN	0	1	↑	0	0	0	1	0	0	1	1	13
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5

6.13 Display On

15H	Display On											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISON	0	1	↑	0	0	0	1	0	1	0	1	15
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Start to display. SLPOUT command must be input before this command. After SLPOUT command, DISON command is waited until “display possible state” and this command is executed after wait time set by PWRCTL command. 											

Display Off

15H	Display On											
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISOFF	0	1	↑	0	0	0	1	0	1	0	1	14
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5

6.14 Page Address Set

25H		Page Address Set										
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PASET	0	1	↑	0	0	1	0	0	1	0	1	25
1st parameter	1	1	↑	PSA7	PSA6	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0	00
2nd parameter	1	1	↑	PEA7	PEA6	PEA5	PEA4	PEA3	PEA2	PEA1	PEA0	9F
3rd parameter	1	1	↑	0	0	0	0	0	0	FrmA1	FrmA0	00
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Set page start address and page end address of display data RAM. PSA: Set page START address PEA: Set page END address FrmA: Set frame address Frame address range set by PASET command is depend on setting of BPPSEL command PSA < PEA 											

6.15 Column Address Set

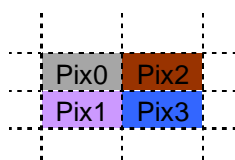
26H		Column Address Set										
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET	0	1	↑	0	0	1	0	0	1	1	0	26
1st parameter	1	1	↑	0	0	0	0	0	0	CSA9	CSA8	00
2nd parameter	1	1	↑	CSA7	CSA6	CSA5	CSA4	CSA3	CSA2	CSA1	CSA0	00
3rd parameter	1	1	↑	0	0	0	0	0	0			02
4th parameter	1	1	↑	CEA7	CEA6	CEA5	CEA4	CEA3	CEA2	CEA1	CEA0	7F
Description	<ul style="list-style-type: none"> Set column start address and column end address of display data RAM. CSA: Set column START address CEA: Set column END address CSA < CEA 											

6.16 Write RAM

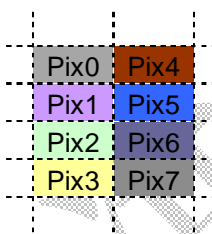
2CH		Write RAM										
Ins/Pat	A1	ERD	RER	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRRAM	0	1	↑	0	0	1	0	0	1	0	0	2C
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Write data	1	1	↑	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0	
Description	<ul style="list-style-type: none"> After this WRRAM command, data is input at display area which is set by CASET and PASET command. RAM address is incremented automatically by WR signal. Column address, page address and frame address are set to start addresses by WRRAM command input. 											

6.17 Addressing

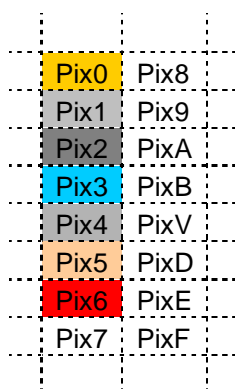
4bpp mode	A1	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DDRAM write command	0	0	0	1	0	1	1	0	0	2C
	1	1	0	0	0	0	1	0	1	00
1 st write	1	Pix13	Pix12	Pix11	Pix10	Pix03	Pix02	Pix01	Pix00	xx
2 nd write	1	Pix33	Pix32	Pix31	Pix30	Pix23	Pix22	Pix21	Pix20	xx



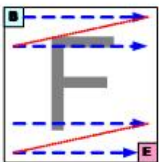
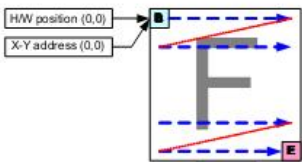
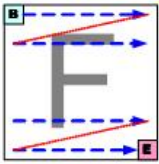
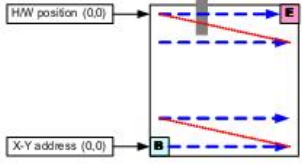
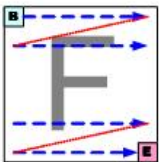
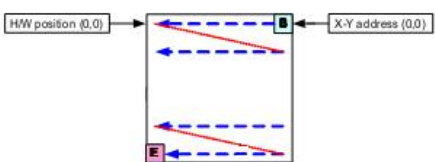
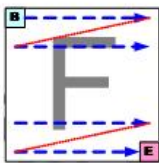
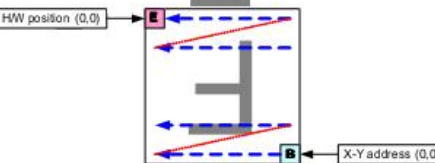
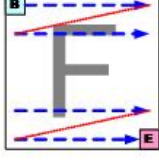
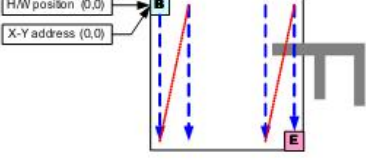
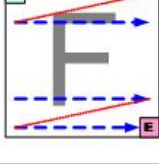
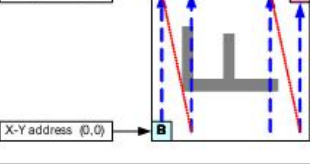
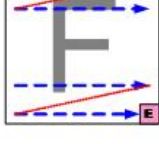
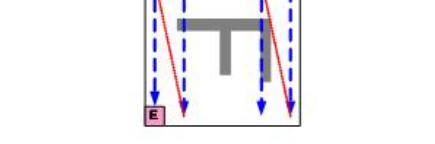
2bpp mode	A1	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DDRAM write command	0	0	0	1	0	1	1	0	0	2C
	1	1	0	0	0	0	1	0	1	00
1 st write	1	Pix31	Pix30	Pix21	Pix20	Pix11	Pix10	Pix01	Pix00	xx
2 nd write	1	Pix71	Pix70	Pix61	Pix60	Pix51	Pix50	Pix41	Pix40	xx

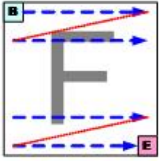
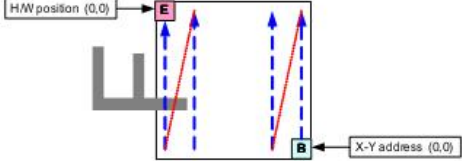


1bpp mode	A1	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DDRAM write command	0	0	0	1	0	1	1	0	0	2C
	1	1	0	0	0	0	1	0	1	00
1 st write	1	Pix7	Pix6	Pix5	Pix4	Pix3	Pix2	Pix1	Pix0	xx
2 nd write	1	PixF	PixE	PixD	PixC	PixB	PixA	Pix9	Pix8	xx



7. Page Address Circuit and Column Address Circuit

Display data direction	Memory access control			Image in the host	Image in the driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		

X-Y Exchange	1	1	1		
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8. Command Table

Instruction	Addr (hex)	A0	END	SWR	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	Function
NOP	00	0	1	1	0	0	0	0	0	0	0	0		Non-Operat ion
SLPOUT	12	0	1	1	0	0	0	1	0	0	1	0		Sleep Out
SLPIN	13	0	1	1	0	0	0	1	0	0	1	1		Sleep In
DISOFF	14	0	1	1	0	0	0	1	0	1	0	0		Display Off
DISON	15	0	1	1	0	0	0	1	0	1	0	1		Display On
DINVOOUT	1A	0	1	1	0	0	0	1	1	0	1	0		Display Invert Out
DINVIN	1B	0	1	1	0	0	0	1	1	0	1	1		Display Invert In
BLOUT	1C	0	1	1	0	0	0	1	1	1	0	0		Blinking Out
BLIN	1D	0	1	1	0	0	0	1	1	1	0	1		Blinking In
STRAME	21	1	1	1	1	0	0	0	0	0	0	1	00	Start Frame Address
BPPSEL	22	1	1	1	1	0	0	0	0	0	0	0	02	BPP Select
MADCTL	24	1	1	1	1	0	0	0	0	0	0	0	00	Memory Address Control
PASET	25	1	1	1	1	0	0	0	0	0	0	0	00	Page Address Set
CASET	26	0	1	1	0	0	0	0	0	0	1	0		Column

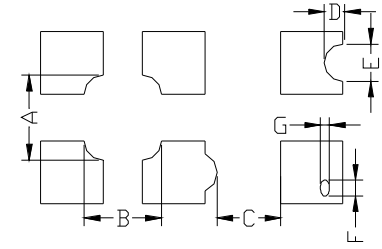
Address Set	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
BLKFIL	CSA8	CSA9	CSA2	CSA3	CSA4	CSA5	CSA6	CSA7	0	0	0	0	0	0	0	0
	CSA0	CSA1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	CEA8	CEA9	CEA2	CEA3	CEA4	CEA5	CEA6	CEA7	0	0	0	0	0	0	0	0
	CEA0	CEA1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BFData0	BFData1	BFData2	BFData3	0	0	0	0	0	0	0	0	0	0	0	0
	00	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
BLSET	BlinkCyc0	BlinkCyc1	BlinkCyc2	BlinkCyc3	BlinkCyc4	BlinkCyc5	BlinkCyc6	BlinkCyc7	0	0	0	0	0	0	0	0
	1D	B2ndF0	B1stF0	B1stF1	0	0	0	0	0	0	0	0	0	0	0	0
	01	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
WRRAM	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RDRAM	DisLin0	DisLin1	DisLin2	DisLin3	DisLin4	DisLin5	DisLin6	DisLin7	0	0	0	0	0	0	0	0
	01	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DISAR	HCIIn0	HCIIn1	HCIIn2	HCIIn3	HCIIn4	HCIIn5	HCIIn6	HCIIn7	0	0	0	0	0	0	0	0
	32	02	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DISSET1	SCIn0	SCIn1	SCIn2	SCIn3	SCIn4	SCIn5	SCIn6	SCIn7	0	0	0	0	0	0	0	0
	0A	28	0C	26	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DISSET2	Part1SL0	Part1SL1	Part1SL2	Part1SL3	Part1SL4	Part1SL5	Part1SL6	Part1SL7	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
PTLSET1	Part2SL8	Part2SL9	Part2SL2	Part2SL3	Part2SL4	Part2SL5	Part2SL6	Part2SL7	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
PTLSET2	Part2SL8	Part2SL9	Part2SL2	Part2SL3	Part2SL4	Part2SL5	Part2SL6	Part2SL7	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0
	00	00	00	00	00	00	00	00	0	0	0	0	0	0	0	0

GATESET	1	1	1	0	Vgck_n2	Vgck_n1	Vgck_n0	0	Vgck_n2	Vgck_n1	Vgck_n0	44
	0	1	1	0	1	1	0	0	1	1	0	00
PWMCTRL	1	1	1	0	VGPP	ScanDir	ScanDir	0	0	0	0	00
	1	1	1	1	0	0	0	0	1	0	1	
	1	1	1	1	0	1	0	0	1	0	1	
	1	1	1	1	0	1	0	0	1	0	1	
	0	1	1	0	1	1	0	1	1	0	0	
	1	1	1	0	0	0	0	0	LEDMD	0	0	
	1	1	1	1	SLED07	SLED06	SLED05	SLED04	SLED03	SLED02	SLED01	SLED00
RDSTAT	1	1	1	1	R16	R15	0	R13	R12	R11	R10	
	1	1	1	0	R26	R25	R24	R23	R22	R21	R20	
	1	1	1	0	R36	R35	R34	R33	R32	R31	R30	
	1	1	1	0	R46	R45	R44	R43	R42	R41	R40	
	1	1	1	0	0	0	0	0	R52	R51	R50	
	1	1	1	0	R66	R65	R64	0	R62	R61	R60	
	0	1	1	0	1	1	1	0	0	1	1	
	1	1	1	1	0	1	0	0	1	0	1	
	1	1	1	1	R17	R15	R14	R13	R12	R11	R10	
	0	1	1	0	1	1	1	0	1	0	1	
RDUID	1	1	1	1	R16	R15	R14	R13	R12	R11	R10	
	1	1	1	1	R26	R25	R24	R23	R22	R21	R20	
	1	1	1	1	R36	R35	R34	R33	R32	R31	R30	
	1	1	1	1	R46	R45	R44	R43	R42	R41	R40	
	1	1	1	1	R56	R55	R54	R53	R52	R51	R50	
	1	1	1	1	R66	R65	R64	R63	R62	R61	R60	
	1	1	1	1	R76	R75	R74	R73	R72	R71	R70	
	1	1	1	1	R86	R85	R84	R83	R82	R81	R80	
	1	1	1	1	R96	R95	R94	R93	R92	R91	R90	
	1	1	1	1	RA7	RA5	RA4	RA3	RA2	RA1	RA0	
	1	1	1	1	RB7	RB5	RB4	RB3	RB2	RB1	RB0	
	1	1	1	1	RC7	RC5	RC4	RC3	RC2	RC1	RC0	
	0	1	1	0	1	1	1	1	0	0	1	
	1	1	1	1	0	1	0	0	1	0	1	
RDVCOMDATA	1	1	1	x	R15	R14	R13	R12	R11	R10		
	1	1	1	x	R25	R24	R23	R22	R21	R20		
	1	1	1	x	R35	R34	R33	R32	R31	R30		
	1	1	1	x	R45	R44	R43	R42	R41	R40		
	1	1	1	x	R55	R54	R53	R52	R51	R50		
	1	1	1	x	R65	R64	R63	R62	R61	R60		
	1	1	1	x	R75	R74	R73	R72	R71	R70		
	1	1	1	x	R85	R84	R83	R82	R81	R80		
	1	1	1	x	RA7	RA6	RA5	RA4	RA3	RA2	RA1	
	1	1	1	x	RB7	RB6	RB5	RB4	RB3	RB2	RB1	

	1	1	1	0	0	0	0	0	0	R63	R62	R61	R60	
GAMSET4 P1	0	1	1	0	0	0	0	0	0	G4BPV03	G4BPV02	G4BPV01	G4BPV00	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BPV04	G4BPV03	G4BPV02	G4BPV01	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BPV14	G4BPV13	G4BPV12	G4BPV11	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BPV24	G4BPV23	G4BPV22	G4BPV21	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BPV34	G4BPV33	G4BPV32	G4BPV31	Gamma Set 4bpp
GAMSET4 P2	0	1	1	0	0	0	0	0	0	G4BPV43	G4BPV42	G4BPV41	G4BPV40	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BPV44	G4BPV43	G4BPV42	G4BPV41	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BPV54	G4BPV53	G4BPV52	G4BPV51	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BPV64	G4BPV63	G4BPV62	G4BPV61	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BPV74	G4BPV73	G4BPV72	G4BPV71	Gamma Set 4bpp
GAMSET4 P3	0	1	1	0	0	0	0	0	0	G4BPV83	G4BPV82	G4BPV81	G4BPV80	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BPV84	G4BPV83	G4BPV82	G4BPV81	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BPV94	G4BPV93	G4BPV92	G4BPV91	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BPV04	G4BPV03	G4BPV02	G4BPV01	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BPV14	G4BPV13	G4BPV12	G4BPV11	Gamma Set 4bpp
GAMSET2 P	0	1	1	0	0	0	0	0	0	G4BPV23	G4BPV22	G4BPV21	G4BPV20	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BPV24	G4BPV23	G4BPV22	G4BPV21	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BPV34	G4BPV33	G4BPV32	G4BPV31	Gamma Set 4bpp
	0	1	1	0	0	0	0	0	0	G2BPV04	G2BPV03	G2BPV02	G2BPV01	Gamma Set 2bpp
	1	1	1	0	0	0	0	0	0	G2BPV14	G2BPV13	G2BPV12	G2BPV11	Gamma Set 2bpp
GAMSET1	0	1	1	0	0	0	0	0	0	G1BPV03	G1BPV02	G1BPV01	G1BPV00	Gamma Set 1bpp
	1	1	1	0	0	0	0	0	0	G1BPV04	G1BPV03	G1BPV02	G1BPV01	Gamma Set 1bpp
	1	1	1	0	0	0	0	0	0	G1BPV14	G1BPV13	G1BPV12	G1BPV11	Gamma Set 1bpp
	1	1	1	0	0	0	0	0	0	G1BNV04	G1BNV03	G1BNV02	G1BNV01	Gamma Set 1bpp
	0	1	1	0	0	0	0	0	0	G1BNV14	G1BNV13	G1BNV12	G1BNV11	Gamma Set 1bpp
GAMSET4 N1	0	1	1	0	0	0	0	0	0	G4BNV03	G4BNV02	G4BNV01	G4BNV00	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BNV04	G4BNV03	G4BNV02	G4BNV01	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BNV14	G4BNV13	G4BNV12	G4BNV11	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BNV24	G4BNV23	G4BNV22	G4BNV21	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BNV34	G4BNV33	G4BNV32	G4BNV31	Gamma Set 4bpp
GAMSET4 N2	0	1	1	0	0	0	0	0	0	G4BNV43	G4BNV42	G4BNV41	G4BNV40	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BNV44	G4BNV43	G4BNV42	G4BNV41	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BNV54	G4BNV53	G4BNV52	G4BNV51	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BNV64	G4BNV63	G4BNV62	G4BNV61	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BNV74	G4BNV73	G4BNV72	G4BNV71	Gamma Set 4bpp
GAMSET4 N3	0	1	1	0	0	0	0	0	0	G4BNV83	G4BNV82	G4BNV81	G4BNV80	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BNV84	G4BNV83	G4BNV82	G4BNV81	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BNV94	G4BNV93	G4BNV92	G4BNV91	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BNV04	G4BNV03	G4BNV02	G4BNV01	Gamma Set 4bpp
	1	1	1	0	0	0	0	0	0	G4BNV14	G4BNV13	G4BNV12	G4BNV11	Gamma Set 4bpp

GAMSET4 N4	9C	G4BNVB5	G4BNVB4	G4BNVB3	G4BNVB2	G4BNVB1	G4BNVB0	2F	
		0	1	1	1	0	0		
		G4BNVC5	G4BNVC4	G4BNVC3	G4BNVC2	G4BNVC1	G4BNVC0	33	Gamma Set
		0	0	0	0	0	0		4ppp
		G4BNVE5	G4BNVE4	G4BNVE3	G4BNVE2	G4BNVE1	G4BNVE0	3B	Negative 4
G4BNVF5	G4BNVF4	G4BNVF3	G4BNVF2	G4BNVF1	G4BNVF0	3F			
GAMSET2 N	9D	G2BNV05	G2BNV04	G2BNV03	G2BNV02	G2BNV01	G2BNV00	00	Gamma Set
		0	0	0	0	0	0		2ppp
		G2BNV15	G2BNV14	G2BNV13	G2BNV12	G2BNV11	G2BNV10	15	Negative
		0	0	0	0	0	0		2A
		G2BNV25	G2BNV24	G2BNV23	G2BNV22	G2BNV21	G2BNV20	2A	
G2BNV35	G2BNV34	G2BNV33	G2BNV32	G2BNV31	G2BNV30	3F			
RMWIN	A1	0	1	0	0	0	0	1	Read Modify
MTPROEN	A2	0	1	0	0	0	0	1	Write In
MTPWREN	A3	0	1	0	0	0	0	1	MTP Read Enable
PTLOUT	A9	0	1	0	0	0	0	1	MTP Write Enable
PTLIN	AA	0	1	0	0	0	0	1	Partial Out
RMWOUT	AC	0	1	0	0	0	0	0	Partial In
SWRESET	AE	0	1	0	0	0	0	0	Read Modify Write Out
		0	1	0	0	0	0	0	Software Reset

8. Inspection Standards

Item	Criterion for defects	Defect type
1) Display on inspection	(1) Non display (2) Vertical line is deficient (3) Horizontal line is deficient (4) Cross line is deficient	Major
2) Black / White spot	Size Φ (mm) Acceptable number $\Phi \leq 0.3$ Ignore (note) $0.3 < \Phi \leq 0.45$ 3 $0.45 < \Phi \leq 0.6$ 1 $0.6 < \Phi$ 0	Minor
3) Black / White line	Length (mm) Width (mm) Acceptable number $L \leq 10$ $W \leq 0.03$ Ignore $5.0 \leq L \leq 10$ $0.03 < W \leq 0.04$ 3 $5.0 \leq L \leq 10$ $0.04 < W \leq 0.05$ 2 $1.0 \leq L \leq 10$ $0.05 < W \leq 0.06$ 2 $1.0 \leq L \leq 10$ $0.06 < W \leq 0.08$ 1 $L \leq 10$ $0.08 < W$ follows 2) point defect Defects separate with each other at an interval of more than 20mm	Minor
4) Display pattern	 $\frac{A+B}{2} \leq 0.28$ $0 < C$ $\frac{D+E}{2} \leq 0.25$ $\frac{F+G}{2} \leq 0.25$ Note: 1) Up to 3 damages acceptable 2) Not allowed if there are two or more pinholes every three-fourth inch.	Minor
5) Spot-like contrast irregularity	Size Φ (mm) Acceptable Number $\Phi \leq 0.7$ Ignore (note) $0.7 < \Phi \leq 1.0$ 3 $1.0 < \Phi \leq 1.5$ 1 $1.5 < \Phi$ 0 Note: 1) Conformed to limit samples. 2) Intervals of defects are more than 30mm.	Minor
6) Bubbles in polarizer	Size Φ (mm) Acceptable Number $\Phi \leq 0.4$ Ignore (note) $0.4 < \Phi \leq 0.65$ 2 $0.65 < \Phi \leq 1.2$ 1 $1.2 < \Phi$ 0	Minor
7) Scratches and dent on the polarizer	Scratches and dent on the polarizer shall be in the accordance with "2) Black/white spot", and "3) Black/White line".	Minor
8) Stains on the surface of LCD panel	Stains which cannot be removed even when wiped lightly with a soft cloth or similar cleaning.	Minor
9) Rainbow color	No rainbow color is allowed in the optimum contrast on state within the active area.	Minor
10) Viewing area encroachment	Polarizer edge or line is visible in the opening viewing area due to polarizer shortness or sealing line.	Minor
11) Bezel appearance	Rust and deep damages that are visible in the bezel are rejected.	Minor
12) Defect of land surface contact	Evident crevices that are visible are rejected.	Minor
13) Parts mounting	(1) Failure to mount parts (2) Parts not in the specifications are mounted (3) For example: Polarity is reversed, HSC or TCP falls off.	Minor
14) Part alignment	(1) LSI, IC lead width is more than 50% beyond pad outline. (2) More than 50% of LSI, IC leads is off the pad outline.	Minor
15) Conductive foreign matter (solder ball, solder hips)	(1) $0.45 < \Phi$, $N \geq 1$ (2) $0.3 < \Phi \leq 0.45$, $N \geq 1$, Φ : Average diameter of solder ball (unit: mm) (3) $0.5 < L$, $N \geq 1$, L: Average length of solder chip (unit: mm)	Minor

16) Bezel flaw	Bezel claw missing or not bent	Minor
17) Indication on name plate (sampling indication label)	(1) Failure to stamp or label error, or not legible.(all acceptable if legible) (2) The separation is more than 1/3 for indication discoloration, in which the characters can be checked.	Minor

深圳鑫洪泰电子

9. Handling Precautions

9.1 Mounting method

A panel of LCD module made by our company consists of two thin glass plates with polarizers that easily get damaged. And since the module is so constructed as to be fixed by utilizing fitting holes in the printed circuit board (PCB), extreme care should be used when handling the LCD modules.

9.2 Cautions of LCD handling and cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

- Isopropyl alcohol
- Ethyl alcohol
- Trichlorotrifluoroethane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Ketene
- Aromatics

9.3 Caution against static charge

The LCD module uses C-MOS LSI drivers. So we recommend you:

Connect any unused input terminal to V_{dd} or V_{ss} . Do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

9.4 Packaging

- Module employs LCD elements, and must be treated as such. Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

9.5 Caution for operation

-It is an indispensable condition to drive LCD module within the limits of the specified voltage since the higher voltage over the limits may cause the shorter life of LCD module.

-An electrochemical reaction due to DC (direct current) causes LCD undesirable deterioration so that the uses of DC (direct current) drive should be avoided.

-Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD module may show dark color in them. However those phenomena do not mean malfunction or out of order of LCD module, which will come back in the specified operating temperature.

9.6 Storage

In the case of storing for a long period of time, the following ways are recommended:

- Storage in polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with not desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping the storage temperature range.
- Storing with no touch on polarizer surface by any thing else.

9.7 Safety

-It is recommendable to crush damaged or unnecessary LCD into pieces and to wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.

-When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well at once with soap and water.

10. Packaging Specifications

	Packaging Specifications HTM062A02	Approved	Checked	Designed

7.1 Packaging Material

No	Item	Dimensions (mm)	1PCS Weight (KG)	Quantity	Total Weight
1	LCM	165.4*92.4*5.8	0.135	56	7.6
2	PE Bag	180*120	0.001	56	0.056
3	Foam Rubber Cushion	310*170	0.0175	4	0.14
4	Partition A1	310*200*100	0.30	4	1.2
5	Product Box	330*180*120 (neutral packing)	0.45	4	1.8
6	Carton	390*370*350 (neutral packing)	0.9	1	0.9
7	Tape			AR	
8	Label Specifications			1	
9	Label Rohs			1	
10	Label ESD			1	

7.2. Total LCD Weight in carton: 11.7 KG ± 10%

7.3. Packaging Specifications and Quantity:

(1) Quantity Of Spacer: A2*6

(2) Total LCM quantity in carton: quantity per box 14* no of boxes 4 = 56

